Amendment to Claims

1 (original). A method for manufacturing an integrated circuit, the method comprising:

(a) forming a plurality of first conductive gates for nonvolatile memory cells, the first conductive gates being spaced from each other and not electrically interconnected;

(b) forming a plurality of conductive floating gates for the memory cells;

(c) forming a plurality of second conductive gates for the memory cells;

(d) forming at least one conductive line electrically interconnecting two or more of the first conductive gates.

2 (original). The method of Claim 1 wherein the first conductive gates are formed before the floating gates and the second conductive gates.

3 (original). The method of Claim 2 wherein the conductive line is formed after the first conductive gates, the floating gates, and the second conductive gates.

4 (original). The method of Claim 1 wherein the conductive line is formed after the first conductive gates, the floating gates, and the second conductive gates.

5 (original). The method of Claim 1 further comprising, after forming the first conductive gates and at least one of the floating gates and the second conductive gates, forming a dielectric to insulate the at least one of the floating gates and the second conductive gates from the conductive line, wherein the dielectric is at least 200 Å thick.

6 (original). The method of Claim 5 wherein the dielectric is at least 500 Å thick.

7 (original). The method of Claim 1 wherein the first conductive gates comprise a semiconductor material, and the conductive line is a metal line.

8 (original). The method of Claim 1 wherein the operation (c) comprises forming at least one conductive line which provides the second conductive gates to at least two adjacent columns of the memory cells.

9 (original). The method of Claim 8 wherein each conductive line formed in the operation (d) interconnects the first conductive gates for at least one row of the memory cells.

10 (original). The method of Claim 1 wherein a plurality of the second conductive gates are interconnected by a conductive line perpendicular to the conductive lines formed in the operation (d).

11 (currently amended). The method of Claim 1 further comprising forming substrate isolation regions in [[the]] a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein the operation (a) comprises forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprises one of the first conductive gates;

wherein the operation (b) comprises:

(b1) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein a maximum distance between points of the adjacent substrate isolation regions above the substrate is not greater than one half of a thickness of the FG layer, and one half of the thickness of the FG layer is smaller than a distance between the adjacent first gate structures; and

(b2) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

12 (currently amended). The method of Claim 1 further comprising forming substrate isolation regions in [[the]] a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein the operation (a) comprises forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprises one of the first conductive gates;

wherein the operation (b) comprises:

(b1) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein the FG layer comprises a planar area between each two adjacent substrate isolation regions and the FG layer comprises a protrusion over each first gate structure; and

(b2) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

13-27 (canceled).

28 (currently amended). A method for fabricating an integrated circuit which comprises nonvolatile memory cells, each memory cell having a conductive floating gate and a first conductive gate insulated from each other, the method comprising:

(a) forming substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

(b) forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure ~~comprising~~ comprises at least one first conductive gate;

(c) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein a maximum distance between points of the adjacent substrate isolation regions above the substrate is not greater than one half of a thickness of the FG layer, and one half of the thickness of the FG layer is smaller than a distance between the adjacent first gate structures;

(d) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

29 (original). The method of Claim 28 wherein the operation (d) is terminated with reference to a time of detecting that the substrate isolation regions have been exposed.

30 (original). The method of Claim 28 wherein each substrate isolation region traverses an array of the memory cells.

31 (original). The method of Claim 28 wherein first gate structures comprise a dielectric over sidewalls of first conductive gates to insulate the first conductive gates from the floating gates.

32 (original). The method of Claim 28 wherein each memory cell further comprises a second conductive gate insulated from the first conductive gate and the floating gate.

33 (original). A method for fabricating an integrated circuit which comprises nonvolatile memory cells, each memory cell having a conductive floating gate and a first conductive gate insulated from each other, the method comprising:

(a) forming substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

(b) forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprising at least one first conductive gate;

(c) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein the FG layer comprises a planar area between each two adjacent substrate isolation regions and the FG layer comprises a protrusion over each first gate structure; and

(d) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

34 (original). The method of Claim 33 wherein the operation (d) is terminated with reference to a time of detecting that the substrate isolation regions have been exposed.

35 (original). The method of Claim 33 wherein each substrate isolation region traverses an array of the memory cells.

36 (original). The method of Claim 33 wherein first gate structures comprise a dielectric over sidewalls of first conductive gates to insulate the first conductive gates from the floating gates.

37 (original). The method of Claim 33 wherein each memory cell further comprises a second conductive gate insulated from the first conductive gate and the floating gate.

38 (new). The method of Claim 5 wherein the dielectric is thicker than a dielectric between a sidewall of said at least one of the floating gates and a sidewall of the first conductive gate of the memory cell comprising the at least one of the floating gates.

39 (new). The method of Claim 1 wherein the integrated circuit comprises a semiconductor substrate, and the first conductive gates are formed over the semiconductor substrate above a top of the semiconductor substrate.

40 (new). The method of Claim 1 wherein:

the integrated circuit comprises one or more conductive lines ("CG lines") each of which provides, and interconnects, a plurality of the second floating gates;

the floating gates are formed before the operation (c); and

the operation (c) comprises:

(c1) forming a layer ("CG layer") over the first conductive gates and the floating gates; and

(c2) lowering an entire top surface of the CG layer at least until the CG layer is removed from over at least portions of the first conductive gates, wherein the remaining CG layer adjacent to the first conductive gates and the floating gates forms the one or more CG lines.

41 (new). The method of Claim 40 further comprising, before operation (c), forming first dielectric between adjacent first conductive gates which are located between future positions of the CG lines;

wherein in (c2), the top surface of the CG layer is lowered to remove the CG layer from over at least a portion of the first dielectric.

42 (new). The method of Claim 41 wherein operation (c) is performed before (d).

43 (new). The method of Claim 41 further comprising forming one or more substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, wherein operation (a) comprises:

(a1) forming a layer ("SG layer") over the semiconductor substrate to provide at least portions of the first conductive gates;

(a2) forming a mask over the SG layer and one or more of the active areas, the mask also overlying one or more of the substrate isolation regions, wherein forming the mask comprises:

forming a first mask over the SG layer to form a pattern identical to a pattern used to define the active areas; and

forming a conformal layer over the first mask and the SG layer and etching the conformal layer to form spacers over sidewalls of the first mask, the mask consisting of the first mask and the spacers;

(a3) etching the SG layer through openings defined by the mask.

44 (new). The method of Claim 44 wherein the first dielectric is formed after (a3) at least in areas from which the SG layer was removed in (a3).

45 (new). The method of Claim 40 wherein the CG layer has a planar top surface at a start of (c2).

46 (new). The method of Claim 40 wherein each CG line provides the second conductive gates to at least two adjacent rows of the memory cells.

47 (new). The method of Claim 1 wherein in each memory cell, each second conductive gate is present over and on a side of a corresponding one of the floating gates.

48 (new). The method of Claim 1 further comprising forming one or more substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, wherein operation (a) comprises:

(a1) forming a layer ("SG layer") over the semiconductor substrate to provide at least portions of the first conductive gates;

(a2) forming a mask over the SG layer and one or more of the active areas, the mask also overlying one or more of the substrate isolation regions, wherein forming the mask comprises:

forming a first mask over the SG layer to form a pattern identical to a pattern used to define the active areas; and

forming a conformal layer over the first mask and the SG layer and etching the conformal layer to form spacers over sidewalls of the first mask, the mask consisting of the first mask and the spacers;

(a3) etching the SG layer through openings defined by the mask.

49 (new). The method of Claim 48 further comprising forming first dielectric at least in areas from which the SG layer was removed in (a3).

50 (new). The method of Claim 48 wherein each substrate isolation region extends in a first direction through an array of the memory cells, and the method further comprises patterning the SG layer using mask strips extending in a second direction through the array, the second direction being transverse to the first direction.

51 (new). The method of Claim 8 wherein each memory cell comprises two of the floating gates.